This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) Method for setting an operating parameter in a peripheral IC, comprising:

transmitting the operating parameter from a central IC via a bus connection to the peripheral IC, the bus connection being a serial bus connection having a data line, a control line, and a clock line;

buffering the operating parameter in a preregister of the peripheral IC, a current operating parameter being stored in a working register of the peripheral IC;

sending a start signal signaling a start of a data transmission via the control line; and

sending a transfer signal from the central IC to the peripheral IC via the control line, the transfer signal triggering transferring of the buffered operating parameter to the working register, wherein the buffered operating parameter becomes active in a working process of the peripheral IC;

wherein the start signal is transmitted on the control line with one of a rising and a falling edge of a system clock signal during a first phase where the system clock signal is present on the clock line and the transfer signal is transmitted on the control line in a second phase where the system clock signal is not present on the clock line.

2. (Cancelled).

3. (Cancelled).

4. (Previously presented) Method according to claim 1, further comprising transferring a register write address for writing to the preregister in the peripheral IC on the data line ahead of the operating parameter.

5. (Cancelled).

6. (Currently amended) A device for setting an operating parameter in a peripheral IC, comprising:

a serial bus connection between a central IC and the peripheral IC, the serial bus connection having a data line, a control line, and a clock line;

means for transmitting the operating parameter from the central IC to the peripheral IC via the serial bus connection;

a preregister for buffering the operating parameter of the peripheral IC;

a working register for storing a current operating parameter of the peripheral IC;

means for transmitting a transfer signal from the central IC to the peripheral IC, the transfer signal triggering transferring of the buffered operating parameter to the working register, wherein the buffered operating parameter becomes active in a working process of the peripheral IC; and

signaling means for transmitting a start signal for data transmission from the central IC to the peripheral IC over the control line;

wherein the start signal is transmitted on the control line with one of a rising or a falling edge of a system clock signal during a first phase where the system clock signal is present on the clock line and the transfer signal is transmitted on the control line in a second phase where the system clock signal is not present on the clock line.

7. (Cancelled).

8. (Cancelled).

9. (Currently amended) Device according to claim 6, further including bus protocol means according to which a register write address for writing to the preregister is transferred to the peripheral IC on the data line ahead of the operating parameter.

10. (Cancelled).

11. (Previously presented) Device according to claim 6, wherein the peripheral IC relates to a front-end IC for a communication arrangement for wireless data transmission and the central IC relates to a signal processing device, with means for one of modulation and demodulation of a mixed RF input signal and for further signal processing in baseband.

12. (Currently amended) Device as claimed in claim 11, wherein the operating parameter relates to a gain setting for a receive gain in the front-end IC.

13. (Previously presented) Device according to claim 6, wherein the device is configured as a send and receive device for wireless data transmission in accordance with the HIPERLAN2 standard.